#19 Appeal Brief
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PATENT
Docket No.: 150.006501

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	B. Vaartstra *et al.*	Group Art Unit:	2815
Serial No.:	09/603,132	Examiner:	E. Lee
Confirmation No.:	3538		
Filed:	23 June 2000		

For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS

APPEAL BRIEF

Assistant Commissioner for Patents
Box AF
Washington, D.C. 20231

Dear Sir:

Applicants present this Appeal Brief in support of the appeal from the final rejection of claims 27-44 as indicated in the Notice of Appeal filed in the above-identified patent application on 25 February 2003.

Real Party In Interest

The real party in interest is Micron Technology, Inc. of Boise, Idaho, as evidenced by the assignment recorded at Reel 9418 Frame 0983 of the parent application (U.S. Serial No. 09/141,240 filed August 27, 1998).

Related Appeals and Interferences

There are no related appeals or interferences pending in connection with any related applications.

Status of Claims

Claims 27-44 are pending. The final rejection of claims 27-44 is appealed. All of pending claims 27-44 are presented in attached Appendix A.

Summary of the Invention

The present invention provides structures that incorporate a diffusion barrier layer formed of chemical vapor deposited $RuSi_x$. The structures incorporating the chemical vapor deposited $RuSi_x$ diffusion barrier layer can include semiconductor device structures, capacitor structures and/or integrated circuit structures.

The semiconductor device structures of the present invention include a substrate assembly having a surface and a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$ over at least a portion of the surface (e.g., a layer formed from Ru and Si precursors). At least a portion of the surface can be a silicon containing surface and the structure can include one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

The capacitor structure of the present invention includes a first electrode, a high dielectric material on at least a portion of the first electrode, and a second electrode on the dielectric material. At least one of the first and second electrodes include a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$ (e.g., a layer formed from Ru and Si precursors). In one example, the first electrode includes the diffusion barrier layer, where the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region. The first electrode can further include one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

The integrated circuit structure according to the present invention includes a substrate assembly having at least one active device and a silicon containing region and an interconnect formed relative to the at least one active device and the silicon containing region. The

interconnect includes a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$ (e.g., a layer formed from Ru and Si precursors) on at least a portion of the silicon containing region. The surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening. The integrated circuit structure can further include a conductive contact material formed relative to the diffusion barrier layer.

Issues

I. Whether claims 27-35 are unpatentable under 35 U.S.C. §102(b) as being anticipated by Matsubara et al. (U.S. Patent No. 5,122,923).

II. Whether claims 27-28, 30-33, and 36-44 are unpatentable under 35 U.S.C. §102(b) as being anticipated by Kuroiwa et al. (U.S. Patent No. 6,239,406).

Grouping of Claims

For the purposes of this appeal, claims 27-44 stand or fall together with respect to Issues I and II identified above.

Arguments

I. Whether claims 27-35 are anticipated under 35 U.S.C. §102(b) by Matsubara et al. (U.S. Patent No. 5,122,923).

Claims 27-35 were rejected under 35 U.S.C. §102(b) as being anticipated by Matsubara et al. (U.S. Patent No. 5,122,923). Applicants respectfully traverse this rejection and request review and reversal by the Board.

Claims 27 and 32

For anticipation under 35 U.S.C. §102, the reference must teach every aspect of the

claimed invention either explicitly or implicitly (M.P.E.P. §706.02). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Matsubara et al. discloses, besides other things, a thin-film capacitor. The thin-film capacitor includes a silicon substrate, an insulating silicon oxide layer, a lower electrode, a dielectric layer of $BaTiO_3$ and an upper electrode of aluminum stacked in sequence from bottom to top (Col. 3, lines 42-47). Matsubara et al. further discloses that the lower electrode layer was formed by a DC magnetron sputtering technique using a target of sintered Ru or $RuSi_2$ (Col. 3, lines 48-56). Thus, Matsubara et al. utilizes a sputtering technique to form the lower electrode layer of $RuSi_2$.

Claims 27 and 32 of the present invention each recite a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$. Matsubara et al. fails to teach a structure that includes a chemical vapor codeposited diffusion barrier layer of $RuSi_x$, as recited in the present invention. In other words, Matsubara et al. describes a sputtered $RuSi_2$ electrode layer and not a chemical vapor codeposited diffusion barrier layer as recited in the present invention.

A diffusion barrier layer formed using chemical vapor deposition as recited in the present invention is different than the layer sputtered according to Matsubara et al. For example, a sputter coated layer, particularly with respect to high aspect ratio structures, provides different coverage thereon when compared to a chemical vapor deposited layer. In contrast, a chemical vapor deposited film provides a highly conformal layer within deep contacts and other openings such as for lower electrodes of storage cell capacitors. *See* Specification, page 9, lines 15-17. These highly conformal layers relative to high aspect ratio structures are generally not possible with sputter coating. Thus, the structures recited in claims 27-35, including chemical vapor codeposited layers, are physically, structurally, and patentably distinct from those recited in

Matsubara et al.

In support of this position, Applicants submit herewith a "Declaration Under 37 C.F.R. §1.132" signed by the inventors (filed in response to the Final Office Action dated 25 November 2002 (included herein as Appendix B)) that states, in part, that there are structural differences between a sputter coated diffusion barrier layer and a chemical vapor deposited diffusion barrier layer. These differences include, but are not limited to, different layer coverage on surfaces having complex geometries. For example, sputter coating a contact hole having a high aspect ratio would typically result in a disproportionately thicker layer of material developing around the opening of the hole as compared to the other surfaces surrounding or within the hole. As a result, the sputter coated diffusion barrier layer may be unable to completely coat the walls and/or the bottom of the contact hole. This would leave regions of the contact hole either not coated or inadequately coated.

In contrast, chemical vapor deposited diffusion barrier layers provide highly conformal and uniform layer coverage on surfaces. This is especially true with respect to surfaces having complex geometries. As such, chemical vapor deposited diffusion barrier layers are more conformal and uniform on surfaces having complex geometries (e.g., openings such as described in claims 39-44) than a sputter coated diffusion barrier layer.

Additionally, structural differences between a sputter coated diffusion barrier layer and a chemical vapor deposited diffusion barrier layer also include differences in the resulting film and substrate qualities. For example, sputter coated diffusion barrier layers can have a high pinhole count as compared to chemical vapor deposited diffusion barrier layers. Also, there is limited stress control possible with sputter coated diffusion barrier layers as compared to chemical vapor deposited diffusion barrier layers.

In addition, an underlying substrate to a sputter coated diffusion barrier layer may have surface damage. This surface damage caused by the sputter coating technique may include implantation of metal into the underlying substrate. For example, ruthenium can be implanted into a silicon substrate surface during the sputter coating of $RuSi_x$. The implanted ruthenium can

then diffuse into the silicon substrate. In addition, silicon can be implanted into platinum surfaces during sputter coating of $RuSi_x$, where the silicon can diffuse into the platinum containing substrate. Either example of diffusion into the underlying substrate provides a structural difference between a sputter coated diffusion barrier layer and a chemical vapor deposited diffusion barrier layer.

As such, sputter coated diffusion barrier layers and chemical vapor deposited diffusion barrier layers have different structures. These differences are such that if a chemical vapor deposited diffusion barrier layer and a sputter coated diffusion barrier layer were analyzed by one skilled in the art they would be able to identify the diffusion barrier layer as either being a sputter coated diffusion barrier layer or a diffusion barrier layer having been deposited by a different technique (e.g., chemical vapor deposited diffusion barrier layer).

The Examiner has asserted, however, that the term "chemical vapor deposited" recites "a method of forming and does not deviate from the structure of a diffusion barrier made of $RuSi_x$." As a result, the Examiner has given no patentable weight to such a term. Applicants traverse this assertion.

Applicants submit that the term "chemical vapor deposited" (which was amended in Applicants' response to the Office Action dated 18 June 2002 to recite "chemical vapor codeposited") is not a "product by process" limitation because the term describes the structure of the barrier layer. *See Hazani v. U.S. Int'l Trade Comm.*, 44 U.S.P.Q.2d 1358, 1363 (Fed. Cir. 2000) (holding that the limitation "chemically engraved" is not a product-by-process limitation).

As stated above, a chemical vapor deposited layer is different than a sputtered layer such as described by Matsubara et al. For example, a chemical vapor deposited layer may be more conformal than a sputtered layer, especially when considering deep contacts and other openings. Further, a chemical vapor deposited layer may exhibit a more uniform distribution of ruthenium and silicide throughout the layer than a layer formed by sputtering or silicidation. Therefore, those skilled in the art would appreciate the structural differences between a chemical vapor deposited layer and a sputtered layer. The words of a claim must be read as they would be

interpreted by those of ordinary skill in the art. *See In re Sneed,* 218 U.S.P.Q. 385 (Fed. Cir. 1983). Those skilled in the art would appreciate that the term "chemical vapor deposited" when used to define a layer describes a structurally different layer than when the term "sputtered" is used to define a layer. As such, the term "chemical vapor codeposited" is not merely a product–by-process limitation and must be given patentable weight in the pending claims.

As a result, Applicants respectfully submit that Matsubara et al. fails to teach all the elements recited in claims 27 and 32 of the present invention. Therefore, such claims are not anticipated by Matsubara et al.

Claims 28-31 and 33-35

Claims 28-31 and 33-35, which depend, either directly or ultimately, from either claim 27 or 32, are not anticipated by Matsubara et al. for the same reasons as presented above for claims 27 and 32. In addition, claims 28-31 and 33-35 each provide additional elements that further support patentability when combined with claims 27 and 32.

For the above reasons, Applicants respectfully submit that claims 27-35 are not anticipated by Matsubara et al. Review and reversal of this rejection are, therefore, respectfully requested.

II. Whether claims 27-28, 30-33, and 36-44 are anticipated under 35 U.S.C. §102(b) by Kuroiwa et al. (U.S. Patent No. 6,239,460).

Claims 27-28, 30-33, and 36-44 were rejected under 35 U.S.C. §102(b) as being anticipated by Kuroiwa et al. (U.S. Patent No. 6,239,460). Applicants respectfully traverse this rejection and request review and reversal by the Board.

Claims 27 and 32

For anticipation under 35 U.S.C. §102, the reference must teach every aspect of the claimed invention either explicitly or implicitly (M.P.E.P. §706.02). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 27 and 32 of the present invention each recite a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$. Kuroiwa et al. discloses, besides other things, a semiconductor device including a capacitor, where a lower electrode of the capacitor is a metal electrode 130 mainly composed of ruthenium or iridium that can be deposited by a chemical vapor deposition process (Abstract and Col. 12, lines 25-35). Kuroiwa et al. provides that when ruthenium is deposited by the chemical vapor deposition process, the raw material may be any one of $Ru(C_5H_5)_2$, $Ru(DPM)_3$, $Ru_3(CO)_{12}$ or $Ru(hfb)(CO)_4$ (Col. 12, lines 43-49). In addition, the metal electrode 130 can be deposited on the top surface of a silicon plug 111, where "a quick heat treatment is performed at 500° C. to 800° C. for 10 seconds to 60 seconds so that a portion of the metal electrode 130 is formed into metal silicide", such as a ruthenium silicide layer (Col. 12, lines 16-27 and Col. 13, lines 7-14). Thus, Kuroiwa et al. utilizes independent deposition steps followed by a heat treatment to form a portion of the metal electrode 130 into ruthenium silicide.

Kuroiwa et al., however, fails to teach a semiconductor device structure that includes a chemical vapor codeposited diffusion barrier layer of $RuSi_x$ over at least a portion of a surface, as recited in claims 27 and 32 of the present invention. In other words, Kuroiwa et al. describes a multi-step process of chemical vapor depositing the metal electrode using materials that do not include silicon, and then heat treating the metal electrode with silicon to form ruthenium silicide. So, unlike the present invention, Kuroiwa et al. teaches forming the ruthenium silicide layer 132

through silicidation, not through chemical vapor deposition. Thus, the teaching of Kuroiwa et al. is in direct contrast to that described in claims 27 and 32 where the $RuSi_x$ is codeposited, i.e., the $RuSi_x$ is deposited by CVD using a ruthenium precursor and a silicon precursor.

Furthermore, one skilled in the art would understand that a codeposited $RuSi_x$ layer exhibits many structural differences over a ruthenium silicide layer formed by silicidation as taught by Kuroiwa et al. For example, a chemical vapor codeposited $RuSi_x$ layer includes a more uniform distribution of silicon throughout the layer, whereas a silicidated ruthenium silicide layer exhibits a gradient of silicon content from the ruthenium/silicon interface to the opposite surface of the ruthenium layer. Further, a silicidated ruthenium silicide layer may include uneven island formations of silicide instead of a more uniform $RuSi_x$ formed by chemical vapor codeposition.

As a result, Applicants respectfully submit that Kuroiwa et al. fails to teach all the elements recited in claims 27 and 32 of the present invention. Therefore, such claims are not anticipated by Kuroiwa et al.

Claims 28, 30-31 and 33

Claims 28, 30-31 and 33 each depend, either directly or ultimately, from one of claims 27 and 32. As such, claims 28, 30-31 and 33 are not anticipated by Kuroiwa et al. for the same reasons as presented above for claims 27 and 32. In addition, claims 28, 30-31 and 33 each recite additional elements that further support patentability when combined with the respective claims 27 and 32 from which they depend.

Claim 36

Claim 36 of the present invention recites an integrated circuit structure that includes an interconnect formed relative to the at least one active device and a silicon containing region, where the interconnect includes a chemical vapor deposited diffusion barrier layer formed of

$RuSi_x$ on at least a portion of the silicon containing region. An interconnect may include, for example, conductive layers in contact holes, vias, etc. *See* Specification, page 1, lines 13-14.

In contrast to claim 36, the embodiment of Kuroiwa et al. relied upon by the Examiner teaches a capacitor structure. *See*, e.g., the Final Office Action dated 25 November 2002, page 2 ("Regarding claims 30-33 and 36-44, Kuroiwa shows (*see*, for example, FIG. 10) a capacitor structure comprising metal electrode (first electrode) 130, capacitor dielectric 115 and upper electrode (second electrode) 116."). In other words, Kuroiwa et al. does not teach an interconnect that includes a chemical vapor deposited diffusion barrier layer.

As a result, Applicants respectfully submit that Kuroiwa et al. fails to teach all the elements recited in claim 36 of the present invention. Therefore, such claim is not anticipated by Kuroiwa et al.

Claim 37

Applicants respectfully submit that Kuroiwa et al. fails to teach every aspect of claim 37. For example, claim 37 recites, in part, that the chemical vapor deposited diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 1 to about 3. Kuroiwa et al. provides a ruthenium silicide layer 132 (Col. 13, lines 7-14). Kuroiwa et al. fails, however, to teach a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 1 to about 3, as recited in claim 37 of the present invention.

As a result, Applicants respectfully submit that Kuroiwa et al. fails to teach all the elements recited in claim 37 of the present invention. Therefore, such claim is not anticipated by Kuroiwa et al.

Claim 38

Claim 38 depends directly from claim 36. As such, claim 38 is not anticipated by Kuroiwa et al. for the same reasons as presented above for claim 36. In addition, claim 38 recites additional elements that further support patentability when combined with claims 36 from

which it depends.

Claims 39-44

Applicants respectfully submit that Kuroiwa et al. fails to teach every aspect of claims 39-44. For example, claims 39 and 41 recite, in part, that the surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening. Kuroiwa et al. provides that a portion of the metal electrode 130 is formed into a ruthenium silicide layer 132 having a film thickness that is preferably 50 nm or thinner (Col. 13, lines 7-15). Kuroiwa et al. fails, however, to teach that the ruthenium silicide layer 132 is on a surface defining an opening as recited in claims 39 and 41 of the present invention, and clearly does not teach that the ruthenium silicide layer 132 is on a surface defining an opening with an aspect ratio greater than 1 as described in claims 40 and 42-44.

As a result, Applicants respectfully submit that Kuroiwa et al. fails to teach all the elements recited in claims 39-44 of the present invention. Therefore, such claims are not anticipated by Kuroiwa et al.

For the above reasons, Applicants respectfully submit that claims 27-28, 30-33, and 36-44 are not anticipated by Kuroiwa et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

Conclusion

Applicants respectfully submit that pending claims 27-44 are patentable. Review and reversal of the rejections are respectfully requested.

Respectfully submitted,

B. Vaartstra *et al.*

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By: _____
Name: Gara Ladwig

APPENDIX A - PENDING CLAIMS ON APPEAL

U.S. Patent Application Serial No.: 09/603,132

Docket No.: 150.00650102

Pending claims 27-44 are reproduced below.

27. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a chemical vapor codeposited diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. The structure of claim 27, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. The structure of claim 32, wherein the first electrode comprises a diffusion barrier layer, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region, and further wherein the first electrode comprises one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. An integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a chemical vapor deposited diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.

38. The structure of claim 36, further comprising a conductive contact material formed relative to the diffusion barrier layer.

39. The structure of claim 27, wherein the surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening.

40. The structure of claim 39, wherein the opening has an aspect ratio greater than about 1.

41. The capacitor structure of claim 32, wherein the capacitor structure includes a surface defining an opening, and wherein the first electrode comprises a diffusion barrier layer formed on the surface defining the opening.

42. The capacitor structure of claim 41, wherein the opening has an aspect ratio greater than about 1.

43. The capacitor structure of claim 42, wherein the opening has an aspect ratio greater than about 1.

44. The capacitor structure of claim 43, wherein the diffusion barrier layer comprises a conformal layer of uniform thickness within the opening.